CLAIMS

1. A method of generating a pulse width modulated (PWM) signal comprising: receiving digital demand data comprising at least one more significant bit (bit_7 to bit_{14}) and at least one less significant bit (bit_0 to bit_6); and generating the PWM signal comprising a sequence of one or more frames (100), each frame (100): comprising a plurality of PWM pulses whose duty cycle is substantially governed by the at least one more significant bit; and having at least one of its PWM pulses selected to have its duty cycle modified in response to the at least one less significant bit, each of the at least one less significant bit uniquely mapping onto the at least one selected PWM pulse of the frame.

2. A method according to Claim 1 where the PWM pulses occur within each frame at a substantially constant pulse repetition frequency.

3. A method according to Claim 1 or 2 wherein the demand data includes one or more data words, each word comprising Q less significant bits bit_i where an index i is in a range of 0 to Q such that bit_0 is the least significant bit, and PWM pulses are selected in each frame at a pulse interval S_p within the frame, the interval S_p being defined by:

$$S_p = \mathrm{INT}\,(2^{Q-i})$$

where INT corresponds to an integer function.

4. A method according to Claim 3 wherein a first pulse S_c in each frame selected to have its duty cycle modified in response to a less significant bit with index i being set is defined by:

$$S_c = \tfrac{1}{2}\, S_p$$

5. A method according to Claim 4 modified so that bit_0 has a first corresponding pulse selected in each frame to be $S_c = S_p$.

6. A method according to Claim 3 wherein each data word comprises 8 more significant bits and 7 less significant bits.

7. Apparatus (10) for generating the PWM signal operable according to the method of any preceding claim, the apparatus (10) including clock means (50) for generating a clock signal for processing according to the method to generate the corresponding PWM signal.

8. Apparatus according to Claim 7 and further comprising switching means (SW1 to SW4) for supplying electrical current to a load (30) in response to the PWM signal.

9. Apparatus according to Claim 8 in which the switching means are coupled in a bridge configuration.

10. Apparatus according to Claim 8 or Claim 9 and further comprising filtering means (L_1, L_2, C_1, C_2) for attenuating relatively higher harmonic components of the PWM signal from reaching the load (30).

11. Apparatus according to Claim 10 in which the filtering means comprises passive components having an impedance which is substantially reactive.

12. Apparatus according to Claim 11 in which the filtering means includes at least one inductor (L_1, L_2) and at least one capacitor (C_1, C_2).

13. Apparatus according to Claim 12 in which the at least one inductor is ferrite cored.

14. Apparatus according to any one of Claims 8 to 13 in which the load comprises a thermo-electric element (30).

15. Apparatus according to Claim 14 in which the element is thermally coupled to one or more of an optical attenuator, a laser and an optical filter for controlling their temperature and thereby their optical characteristics.

16. An optical attenuator (200) for receiving input radiation (P_i) and attenuating the input radiation (P_i) to provide corresponding output radiation (P_o) comprising: attenuating means (210) for receiving the input radiation (P_i) and attenuating the input radiation (P_i) to provide the output radiation (P_o) in response to a drive signal; said attenuating means being operable to provide an attenuation dependent upon its temperature; the attenuating means including temperature modifying means (30) for modifying its temperature in response to the drive signal and controlling means (10) for receiving a signal (P_R) indicative of attenuation required and for generating the corresponding drive signal characterised in that the drive signal is derived from a PWM signal in which each PWM signal cycle corresponds to a frame, a plurality of such successive forming a multiframe and the controlling means being operable to modify the duty ratio of one or more frames within each multiframe for providing enhanced resolution attenuation provided by the attenuator.

17. An attenuator according to Claim 16 in which the PWM signal is of substantially constant cycle period (t_0), and further comprising filtering means (260) operable to attenuate PWM signal components at a frequency corresponding to the cycle period.

18. An attenuator according to Claim 16 or Claim 17 in which modifications to the duty ratio of frames within each multiframe are substantially uniformly distributed within the multiframe (Table 6).

19. An attenuator according to Claim 17 in which the duty ratio of each frame is incrementable in discrete steps, the modifications to the duty ratio of the frames corresponding to one such step difference.

20. An attenuator according to any one of Claims 16 to 19 in which each multiframe comprises in a range of 2 to 1000 frames.

21. An attenuator according to Claim 20 in which each multiframe comprises 64 frames.

22. An attenuator according to any one of Claims 16 to 21 and further comprising: detecting means (230) for receiving a portion of the output radiation (P_o) and generating a corresponding detection signal (T_1); amplifying means within the controlling means (10) for comparing the detection signal (T_1) with a reference signal (P_R) and for adjusting via the temperature modifying means (30) the temperature of the attenuating means (210) so that the output radiation (P_o) has associated therewith a radiation power determined by the reference signal (P_R).

23. An attenuator according to any one of Claims 16 to 22 in which the controlling means (10) is implemented as a field programmable gate array (FPGA) (240).

24. An attenuator according to Claim 23 in which the FPGA is operable to generate a PWM signal which is buffered by power MOSFETs (FET1, FET2) for output to drive the attenuating means.

25. An attenuator according to Claim 23 or Claim 24 in which the FPGA is clocked at a rate of at least 30 MHz.